[혼성모드 및 데이터 컨버터 집적회로]

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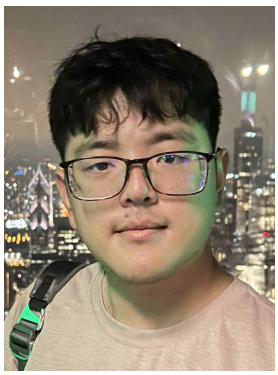
| 초청연사 1 |  |
| | 이승종 Staff Engineer<br>(Qualcomm) |
| 제 목 | Timing optimization on CT-DT hybrid SDM |
| 요약문 | Continuous-time Sigma Delta Modulators (CT SDMs) offer advantages over discrete-time designs, including easier input drive and lower power consumption due to the absence of switched-capacitor integrators. These benefits have driven significant research into CT SDMs in recent years. Traditionally, SDMs have employed flash-type quantizers, but there is growing use of successive approximation register (SAR) quantizers, which enable higher resolution and lower power consumption. In particular, Noise-Shaped (NS) SAR quantizers are utilized in high-performance SDM implementations, providing an additional noise shaping order. In this presentation, we will review the internal timing of SDMs when using NS SAR quantizers and discuss an optimized SDM architecture. |
| 초청연사 2 |  |
| | 창동진 교수<br>(충남대 전자공학과) |
| 제 목 | A Key Building Block of AI Accelerator: In-Memory Computing Macros |
| 요약문 | Static random-access memory (SRAM) or register is an essential building block for implementing digital systems. The development of artificial neural networks for artificial intelligence (AI) has led to algorithms that require many |

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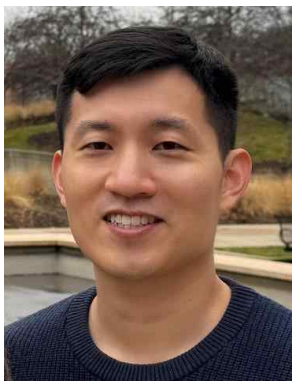
| | iterations of simple operations especially, matrix multiplication. These characteristics of these computations led to trends of hardware, which supports highly parallel computation. With these trends, SRAM/register in-memory computing (IMC) macros for accelerating neural networks have been popularly researched in recent years. Besides, the research for IMC macros becomes enlarged from macros to systems that consider the data movement among IMC macros. Since data movement among IMC macros can be reduce the access number of conventional SRAM, the power efficient computation and high throughput can be achieved for the systems. In this talk, the review for the latest trend in IMC macros are discussed and the issue for the future research is proposed. |
| 초청연사<br>3 |  |
| | 강태욱 교수<br>(성균관대학교 반도체융합공학과) |
| 제 목 | AI Sensor system IC |
| 요약문 | With the rise of AI technology, mixed-signal sensor systems are leveraging AI integration to enhance their capabilities. This presentation will examine recent research trends in sensor systems, which typically consist of analog-to-digital converters (ADC), digital signal processors, and AI engines. Key areas of focus include very-large-scale mixed systems, compact form factors, adaptive functionalities, and AI-driven applications. The talk will also present research on an acoustic beamformer system IC and highlight essential design considerations for speech recognition systems, which demand both analog and digital design techniques. |