[Advanced Logic, Memory, and Interconnect Device Technologies]

초청연사 1	
	이철호 교수 (서울대 전기정보공학부)
제 목	Interface Band Engineering for High-Performance 2D Semiconductor Electronics
요약문	Two-dimensional (2D) semiconductors such as transition metal dichalcogenides (TMDs) have emerged as promising materials for implementing beyond-CMOS electronics due to excellent gate coupling and immunity to short-channel effects at the ultimate scaling. In addition, owing to a van der Waals layered structure, they hold great potential for non-conventional electronics capable of heterogeneous integration and deformation. To achieve high-performance 2D field-effect transistors (FETs), it is highly required to control the electronic states and energy band profiles at various heterointerfaces among the semiconductor channel, the gate dielectric, and metal electrodes. In this talk, I will present two types of proof-of-concepts 2D FETs enabled by interface band engineering: 1) modulation-doped FETs (MODFETs) and 2) metal-semiconductor FETs (MESFETs). In a MODFET, we demonstrated remote modulation doping in the type-II band-modulated channel, enabling us to achieve high mobility by suppressing dopant-induced charge impurity scattering. The 2D MESFETs were also demonstrated using the Fermi-level pinning-free metal Schottky gate, whose device characteristics approach the Boltzmann switching limit.
초청연사 2	

	
	허근 교수 (전북대 반도체과학기술학과)
제 목	Overcoming the Limitation of Cell Transistor in Ultimately Scaled Memory
요약문	With the advent of the IoT era, the demand for high-performance memory that can store and utilize a wider bandwidth of information more efficiently is continuously increasing. However, due to the quantum mechanical limitations of device scaling, an important innovation such as vertical 3D stacking is now desperately needed. Under these technical circumstances, we propose a methodology to fundamentally overcome the limitations of scaling through material and structural innovations. We investigated the electrical performance of a second-order vertical structured 3D memory cell repeatedly composed of vdW channel and high-k gate dielectric. The fabricated vdW FETs were used as access transistors of the 3D memory. Atomically thin, dangling bond-free vdW TMDs are known as next-generation semiconductor materials that can effectively suppress SCE. TCAD and high-frequency structural simulations were performed for the optimal design. In addition, the read/write, pre-charge operation and electrical performances were thoroughly analyzed through mixed-mode simulations.
초청연사 3	
	조성재 교수 (이화여대 융합전자반도체공학부)
제 목	Ultra-fast and Ultra-low-power Group-IV Optical

	Interconnect Devices
요약문	Through the incessant scaling down of transistors, various goals such as higher integration density, reduced power consumption per transistor, increased data processing speed, and multifunctionality of chips of the same size have been plausibly achieved. However, near the end of 20th century, the limits of improving processing speed of central processing unit (CPU) by making transistors smaller were already reached, and the speed of systems is governed by the tremendous RC delay from the exponentially increased metal wires. In this talk, optical interconnect device technologies based on group-IV semiconductors will be explored. We will review the theoretical background of photon-particle interaction within semiconductors and look into the development results of key technologies such as photodetectors, cavities, light source, and electro-optical transistors based on group-IV semiconductors that are compatible with CMOS processes. Also, examining technology trends, the technical issues and the directions that need to be considered will be surveyed.