Experimental investigation of physical mechanism for asymmetrical degradation and related noise properties in a-IGZO TFTs under simultaneous gate and drain bias stresses

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We experimentally investigate the physical mechanism for asymmetrical degradation in amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) under simultaneous gate and drain bias stresses. The transfer curves exhibit an asymmetrical negative shift after the application of gate-to-source (V_{GS}) and drain-to-source (V_{DS}) bias stresses of (V_{GS}=24 V, V_{DS}=15.9 V) and (V_{GS}=22 V, V_{DS}=20 V), but the asymmetrical degradation is more significant after the bias stress (V_{GS}, V_{DS}) of (22 V, 20 V) nevertheless the vertical electric field at the source is higher under the bias stress (V_{GS}, V_{DS}) of (24 V, 15.9 V) than (22 V, 20 V). By using the modified external load resistance method, we extract the source contact resistance (R_S) and the voltage drop at R_S ($V_{S,\,drop}$) under both stress conditions, and discuss the physical mechanism causing the observed phenomenon based on the obtained results. We also investigate the low-frequency noise (LFN) properties under various bias and temperature stress conditions. The LFNs measured before and after the stresses are well-fitted using the correlated number fluctuation-mobility fluctuation (Δn-$\Delta\mu$) model, and we extracted values of the border trap density (N_T) and the Coulomb scattering coefficient (α_S). After application of a gate bias stress, the LFN properties hardly change. However, the LFN increases after application of simultaneous gate and drain bias stresses. In addition, the increase in temperature during application of the simultaneous gate and drain bias stresses accelerates the increase of LFN after the stress.

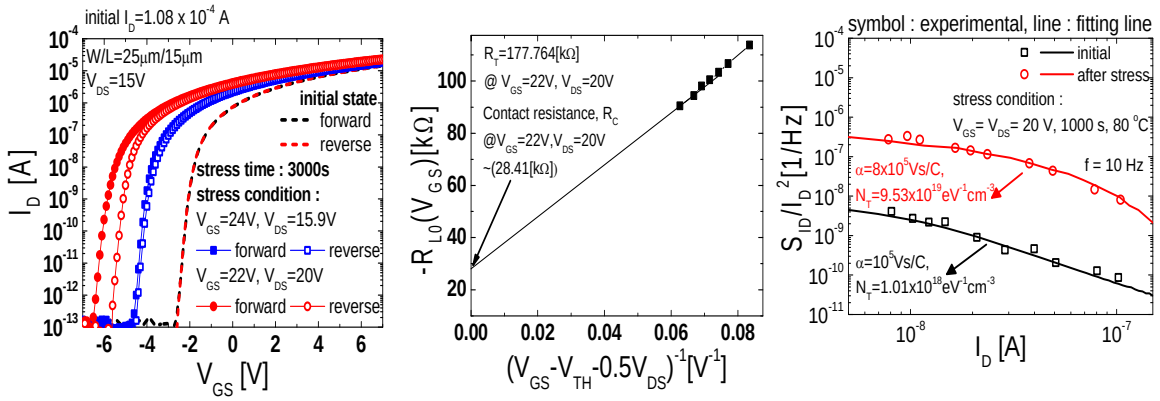

Fig 1. Change of transfer curves, voltage drop at $R_{S,}$ and LFN properties in a-IGZO TFT after simultaneous gate and drain bias stresses.

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